

D:wave

QUANTUM REALIZED.



Quantum Circuits, Inc.

FORWARD LOOKING STATEMENT



Certain statements in this presentation are forward-looking, as defined in the Private Securities Litigation Reform Act of 1995, including statements relating to the acquisition (including the timing and completion thereof), as well as the combined company's development and commercialization plans, plans to accelerate the projected time to a scaled, error-corrected gate model quantum computer and intention to make an initial dual-rail system generally available in 2026, among others. In some cases, you can identify forward-looking statements by the following words: "believe," "may," "will," "could," "would," "should," "expect," "intend," "plan," "anticipate," "trend," "believe," "estimate," "predict," "project," "potential," "seem," "seek," "future," "outlook," "forecast," "projection," "continue," "ongoing," or the negative of these terms or other comparable terminology, although not all forward-looking statements contain these words. These statements involve significant risks, uncertainties, and other factors that may cause actual results to differ materially from the information expressed or implied by these forward-looking statements and may not be indicative of future results. These forward-looking statements are subject to a number of risks and uncertainties, including, among others, various factors beyond management's control, including the risks set forth under the heading "Risk Factors" discussed under the caption "Item 1A. Risk Factors" in Part I of our most recent Annual Report on Form 10-K or any updates discussed under the caption "Item 1A. Risk Factors" in Part II of our Quarterly Reports on Form 10-Q and in our other filings with the SEC. Undue reliance should not be placed on the forward-looking statements in this presentation in making an investment decision, which are based on information available to us on the date hereof. We undertake no duty to update this information unless required by law.



D-Wave Is Now
The World's Leading
Quantum Computing Company

DIFFERENTIATED DUAL-PLATFORM STRATEGY

Annealing & Gate



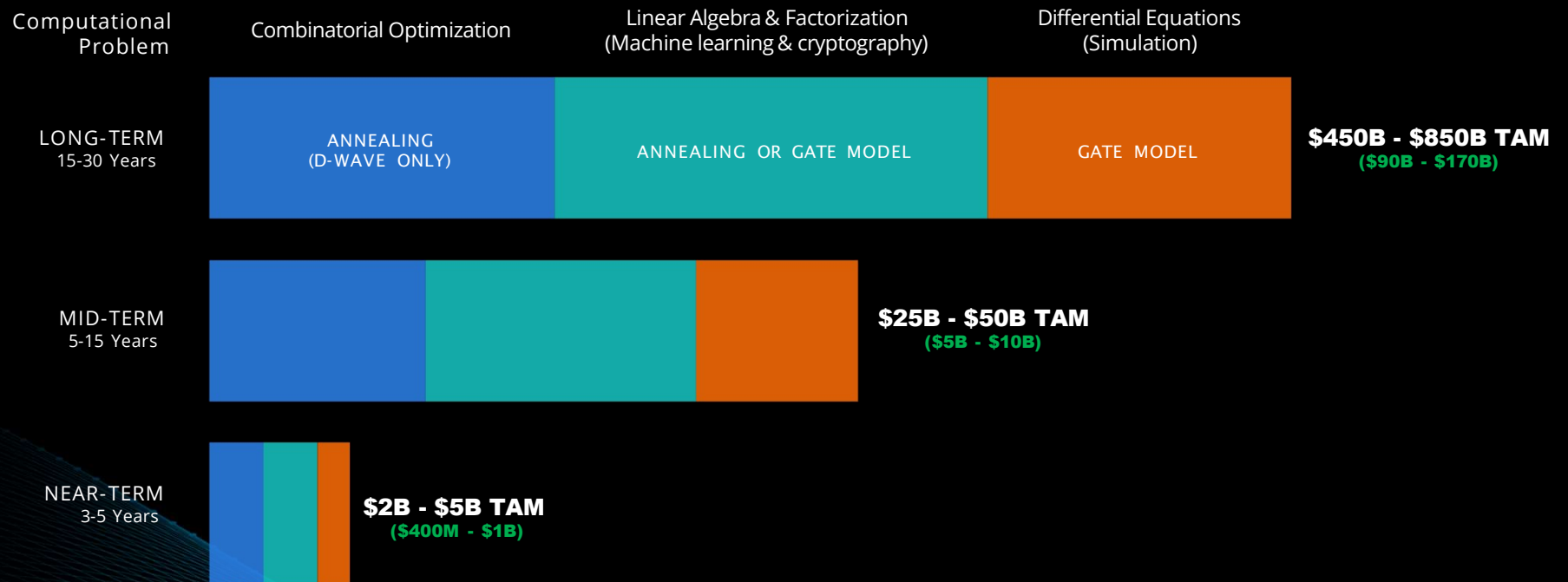
Full TAM

Secures D-Wave's position as only company capable of addressing full quantum computing addressable market with industry-leading gate-model and annealing quantum computing technology

Value to Customers

Customers will need annealing AND gate-model systems to solve the full breadth of computational problems, and D-Wave is uniquely positioned to deliver

D-WAVE NOW ENABLES ACCESS TO THE FULL QUANTUM TAM¹



¹ Boston Consulting Group: "Where Will Quantum Computers Create Value – and When?" May 2019 (80% of TAM accruing to end-users; 20% to quantum hardware, software and services providers)

EXTENDING D-WAVE MARKET LEADERSHIP POSITION



Dual-platform Approach

Only company delivering both annealing and gate-model systems addressing full range of customer problems

Beyond Classical

Only company that's demonstrated quantum supremacy on a real-world problem (Annealing)

Production-grade & In-use

Only company with customer applications in production (Annealing)

Built-in Error Correction

Unique dual-rail technology needed to efficiently error-correct gate systems

On-chip Control

Local cryogenic control and multi-chip superconducting packaging for efficient scaling

Significant Talent & IP

Doubled size of world-class quantum team, with Quantum Circuits' esteemed quantum scientists and developers



DIFFERENTIATED TECHNOLOGY FOR OPTIMIZATION

ANNEALING'S LONG TERM ADVANTAGE IN OPTIMIZATION

OPTIMIZATION IS A KEY APPLICATION AREA FOR ANNEALING QUANTUM COMPUTING



- More resilient to errors
- Does not require significant preprocessing or tuning
- Does not require high bandwidth qubit control
- Technology is scaling to thousands of qubits
- Near-term large-scale quantum computing technology

ANNEALING'S LONG TERM ADVANTAGE IN OPTIMIZATION



Empirical benchmarking shows NISQ gate-model systems cannot compete with annealing on time, accuracy, or problem scale

Even after scaled error-corrected gate-model systems are developed, they will not compete in optimization

Article | [Open access](#) | Published: 12 March 2024

Short-depth QAOA circuits and quantum annealing on higher-order ising models

[Elijah Pelofske](#) , [Andreas Bärtzsch](#)  & [Stephan Eidenbenz](#)

[npj Quantum Information](#) **10**, Article number: 30 (2024) | [Cite this article](#)

2127 Accesses | 3 Altmetric | [Metrics](#)

Focus beyond Quadratic Speedups for Error-Corrected Quantum Advantage

Ryan Babbush, Jarrod R. McClean, Michael Newman, Craig Gidney, Sergio Boixo, and Hartmut Neven
PRX Quantum **2**, 010103 – Published 29 March 2021

ANNEALING'S LONG TERM ADVANTAGE IN OPTIMIZATION

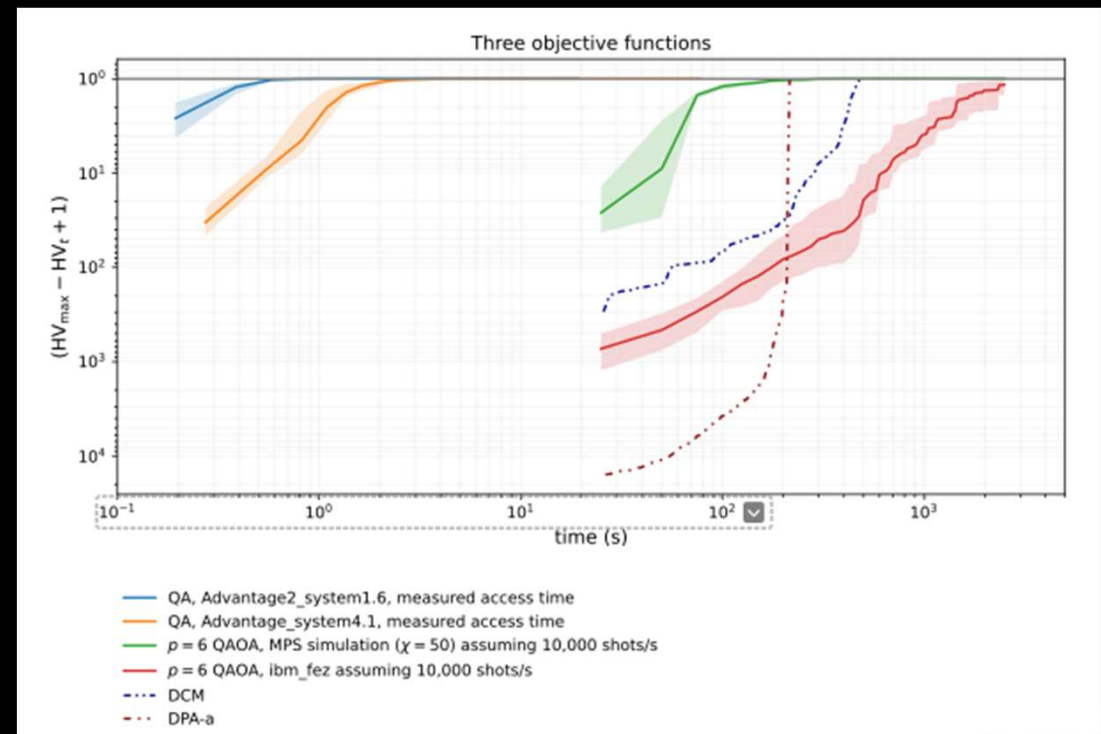


Multi-objective optimization by quantum annealing

Andrew D. King¹

¹D-Wave Quantum Inc., 3033 Beta Ave., Burnaby, BC, Canada
(Dated: November 4, 2025)

> 1000x performance differential between Advantage™ annealing systems and IBM gate-model system in multi-objective optimization



CAN GATE-MODEL QUANTUM COMPUTING SYSTEMS EMULATE ANNEALING QC SYSTEMS? **NO.**



- In principle, gate-model systems can simulate annealing systems
- In practice, the classical overhead is prohibitive - even for very simple systems!
- This analysis does not even account for the classical overhead involved with error correction

The Cost of Emulating a Small Quantum Annealing Problem in the Circuit-Model

Javier Gonzalez-Conde,^{1,2,*} Zachary Morrell,³ Marc Vuffray,⁴ Tameem Albash,⁵ and Carleton Coffrin^{3,†}

¹*Department of Physical Chemistry, University of the Basque Country UPV/EHU, Apartado 644, 48080 Bilbao, Spain*

²*EHU Quantum Center, University of the Basque Country UPV/EHU, Apartado 644, 48080 Bilbao, Spain*

³*Advanced Network Science Initiative, Los Alamos National Laboratory Los Alamos, NM 87545, USA*

⁴*Theoretical Division, Los Alamos National Laboratory Los Alamos, NM 87545, USA*

⁵*Center for Computing Research, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA*

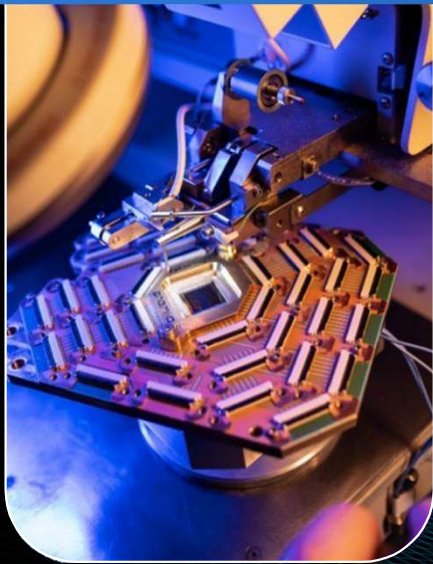
(Dated: February 28, 2024)

Demonstrations of quantum advantage for certain sampling problems has generated considerable excitement for quantum computing and has further spurred the development of circuit-model quantum computers, which represent quantum programs as a sequence of quantum gates acting on a finite number of qubits. Amongst this excitement, analog quantum computation has become less prominent, with the expectation that circuit-model quantum computers will eventually be sufficient for emulating analog quantum computation and thus rendering analog quantum computation obsolete. In this work we explore the basic requirements for emulating a specific analog quantum computation in the circuit model: the preparation of a biased superposition of degenerate ground states of an Ising Hamiltonian using an adiabatic evolution. We show that the overhead of emulation is substantial even for this simple problem. This supports using analog quantum computation for solving time-dependent Hamiltonian dynamics in the short and mid-term, assuming analog errors can be made low enough and coherence times long enough to solve problems of practical interest.

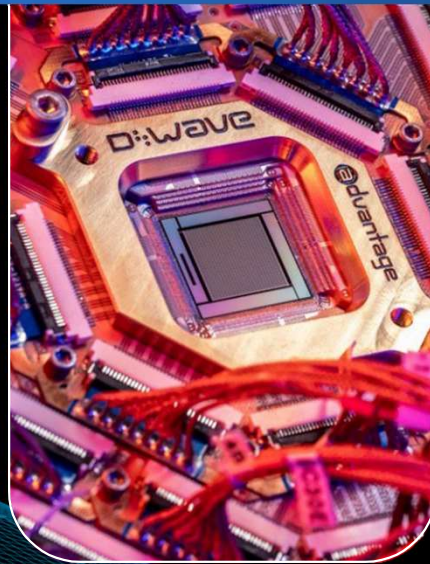
ADVANTAGE3™ SYSTEM: 100,000 QUBIT ANNEALING QUANTUM COMPUTER



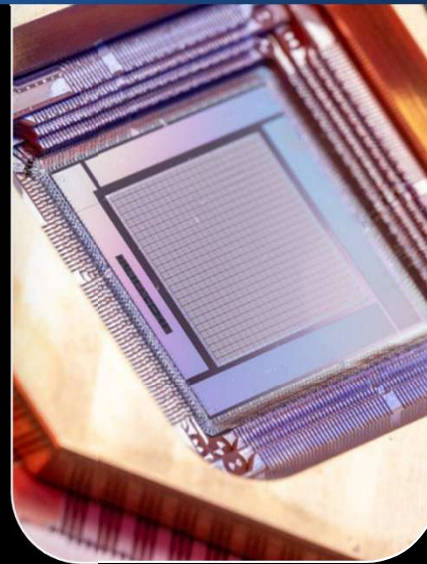
Increasing connectivity and coherence



Next generation digital addressing



Increasing scale through multi-chip processor fabrics



Larger scale cryogenic enclosure





DIFFERENTIATED TECHNOLOGY FOR ERROR CORRECTION AND SCALE

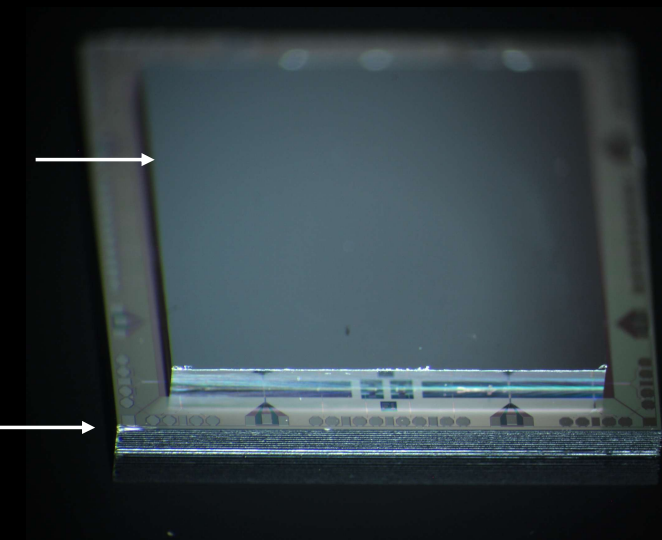
SCALABLE, ON-CHIP CONTROL OF GATE-MODEL QUBITS



- Validated that the on-chip cryogenic control technology D-Wave developed for its commercial annealing quantum processing units can also be applied to its gate model architectures
- Annealing control technology uses multiplexed digital-to-analog converters to control tens of thousands of qubits and couplers with just 200 bias wires
- The same control technology can reduce gate-model wiring complexity while maintaining qubit fidelity – which enables large-scale, practical gate model QPUs

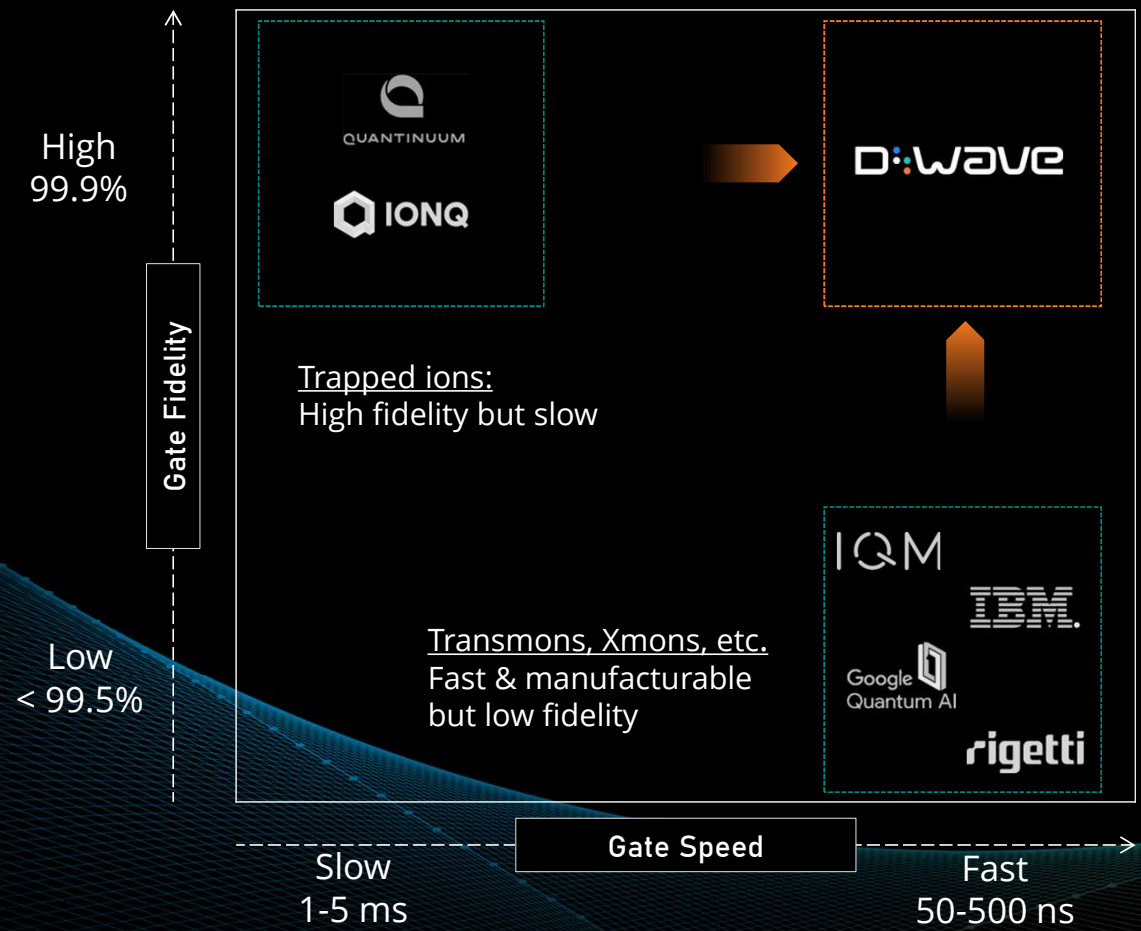
High fidelity
qubit chip

Scalable
control chip



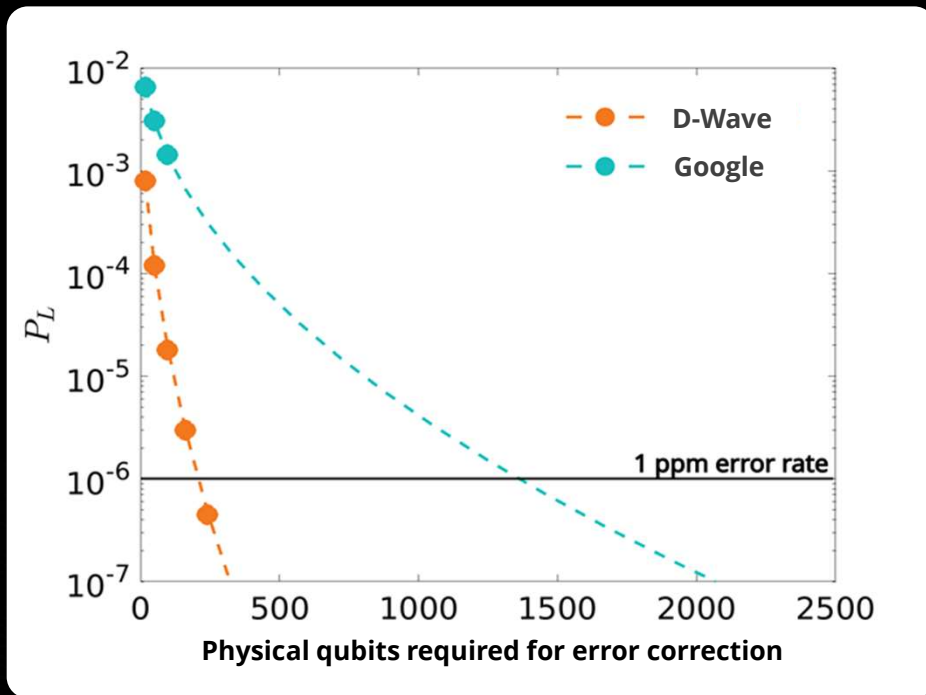
GATE MODEL GAME CHANGER

Superconducting Speed With Ion Trap Fidelity

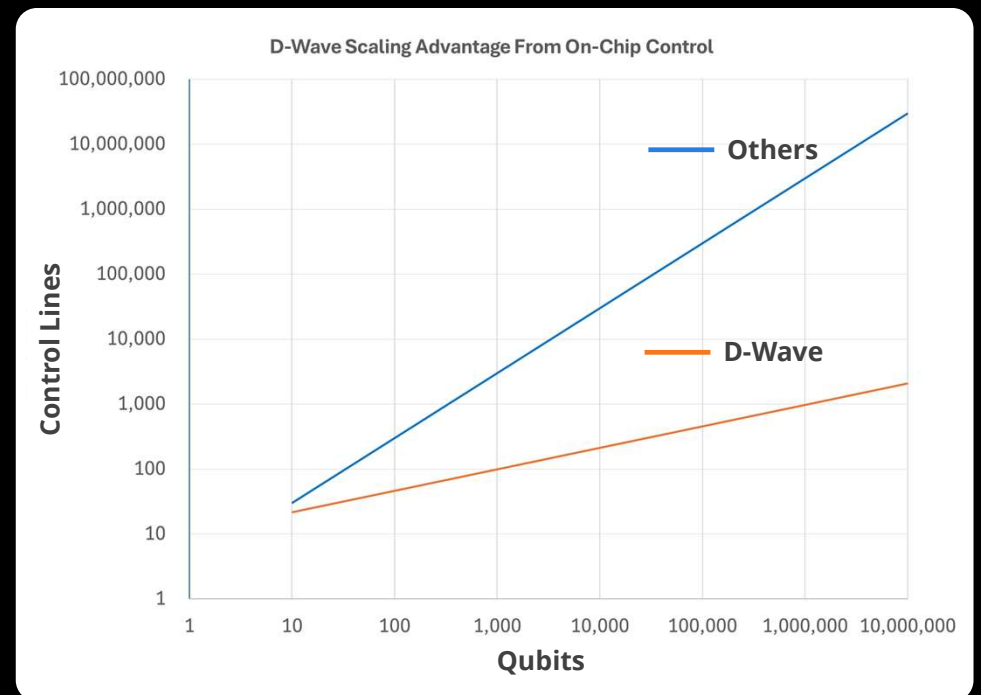


Inherent error detection in dual-rail qubits drives leading gate fidelities (99.9%+)

DUAL-RAIL QUBITS OFFER FASTER PATH TO ERROR CORRECTION; ON-CHIP CONTROL UNLOCKS SCALE



Up To 10x Reduction In Physical Qubits Required
For Error-Corrected Logical Qubits

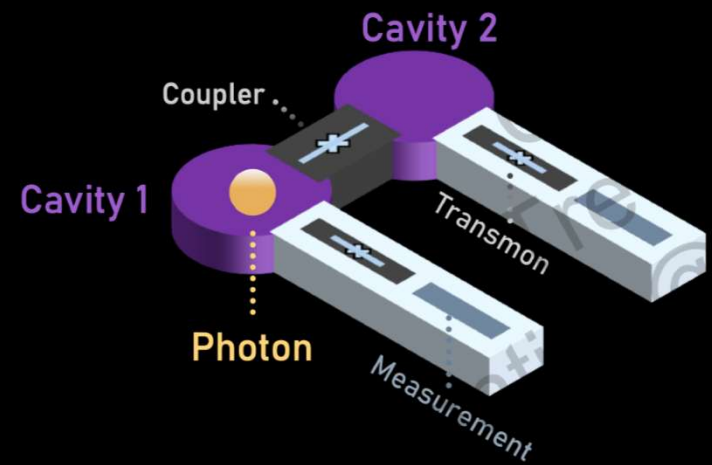


On-chip Control Reduces Qubit Control Line Count
By Orders of Magnitude

INITIAL DUAL-RAIL SYSTEM GENERALLY AVAILABLE IN 2026



- Aqumen Seeker™ dual-rail processor currently operational for alpha users
- Installed at Quantum Circuits' laboratory in New Haven, Connecticut
- Universal gate set available with gate speeds up to 1000x faster than neutral atom and trapped ion technology
- Built in quantum error detection enables early algorithm development
- Valuable industry-leading platform for research focused organizations and HPCs exploring error correction and QPU integration



THREE YEAR GATE-MODEL ROADMAP

Build and Commercialize Error-Corrected Superconducting Gate-Model Processors



2026

- General availability of 17 qubit dual-rail transmon-based system along with error correction demonstration
- Dual-rail solvers available in Leap™ cloud platform
- Release software toolkit for quantum algorithm development

2027

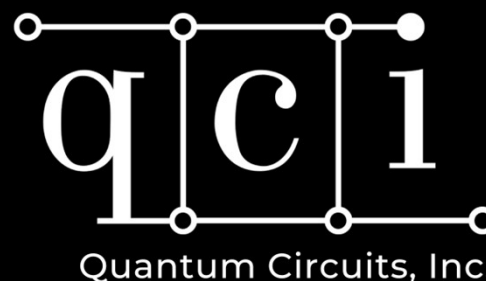
- General availability of 49 qubit dual-rail transmon-based system
- Complete initial build of 181 qubit dual-rail transmon-based processor

2028

- General availability of 181 qubit dual-rail transmon-based system
- Error correction demonstration with multiple logical qubits
- High fidelity gate operations on scalable logical qubits
- Design for 1,000 qubit scalable dual-rail processor completed



Commercial-Grade | Groundbreaking Science | Unparalleled Technical Leadership



**Today: First to market with a commercial, beyond classical
(Annealing) quantum computer**

**Tomorrow: First to market with a scaled, error-corrected
(Gate-Model) quantum computer**