SYNOPSYS®

These Prepared Remarks contain forward-looking statements, including, but not limited to, statements regarding Synopsys, Inc.'s ("***Synopsys***", "***our***" or "***we***") short-term and long-term financial targets, expectations and objectives; strategies related to our products, technology and services; business and market outlook, opportunities, strategies and technological trends, such as artificial intelligence; our pending acquisition of ANSYS, Inc. (the "***Ansys Merger***"), including, among other things, expectations regarding the financing of the pending acquisition; the exploration of strategic alternatives for our Software Integrity segment; the potential impact of the uncertain macroeconomic and geopolitical environment on our financial results; the expected impact of U.S. and foreign government actions and regulatory changes, including export control restrictions, on our financial results; customer demand and market expansion; our planned product releases and capabilities; industry growth rates; the expected realization of our contracted but unsatisfied or partially unsatisfied performance obligations (backlog); software trends; planned stock repurchases; our expected tax rate; and the impact and result of pending legal, administrative and tax proceedings. These statements involve risks, uncertainties and other factors that could cause our actual results, time frames or achievements to differ materially from those expressed or implied in such forward-looking statements. Such risks, uncertainties and factors include, but are not limited to: macroeconomic conditions and geopolitical uncertainty in the global economy; uncertainty in the growth of the semiconductor and electronics industries; the highly competitive industry we operate in; actions by the U.S. or foreign governments, such as the imposition of additional export restrictions or tariffs; consolidation among our customers and our dependence on a relatively small number of large customers; risks and compliance obligations relating to the global nature of our operations; failure to complete the Ansys Merger on the terms described in our filings with the SEC, if at all; failure to obtain required governmental approvals related to the Ansys Merger or the imposition of conditions to such governmental approvals that may have an adverse effect on us; failure to realize the benefits expected from the Ansys Merger; and more. Additional information on potential risks, uncertainties and other factors that could affect Synopsys' results is included in filings we make with the Securities and Exchange Commission (the "***SEC***") from time to time, including in the sections entitled "Risk Factors" in our latest Annual Report on Form 10-K and in our latest Quarterly Report on Form 10-Q. The financial information contained in these Prepared Remarks should be read in conjunction with the consolidated financial statements and notes thereto included in Synopsys' most recent reports on Forms 10-K and 10-Q, each as may be amended from time to time. Synopsys' financial results for its first quarter of fiscal year 2024 are not necessarily indicative of Synopsys' operating results for any future periods. The information provided herein is as of February 21, 2024. Although these Prepared Remarks are expected to remain available on Synopsys' website through the date of the earnings results call for the second quarter of fiscal year 2024, their continued availability through such date does not mean that Synopsys is reaffirming or confirming their continued validity. Synopsys undertakes no duty, and does not intend, to update any forward-looking statement, whether as a result of new information, future events or otherwise, unless required by law.

These Prepared Remarks also contain non-GAAP financial measures as defined by the SEC in Regulation G. Reconciliations of certain non-GAAP financial measures to their most closely applicable GAAP measures are included in the first quarter fiscal year 2024 earnings release and financial supplement, each dated February 21, 2024 and available on Synopsys' website at www.synopsys.com. Additional information about such reconciliations can be found in Exhibit 99.1 of Synopsys' Current Report on Form 8-K, filed with the SEC on February 21, 2024.

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Good afternoon. In Q1, we continued our strong momentum with revenue in the upper end of our guidance range and non-GAAP EPS surpassing the upper end of our guidance range. Revenue was $1.65 billion, up 21% year-over-year, non-GAAP operating margin was 38.7%, up approximately 3.5 points year-over-year, non-GAAP EPS was $3.56, up 36% year-over-year. While maintaining our laser focus on meeting our quarterly financial commitments, we strategically drive the business for long-term financial success. Over the last three years, we have delivered a 17% revenue CAGR, non-GAAP operating margin improvement of 7 points, and non-GAAP EPS growth at a 26% CAGR. Shelagh will discuss the financials and guidance in more detail.

Let's turn to market trends. We have entered an era of pervasive intelligence, driven by the rise of artificial intelligence, silicon proliferation, and software-defined systems. These trends demand more compute, new architectures, and new design methodologies, while requiring us to address the significant challenges of complexity, cost, energy consumption and security. Despite the mounting challenges, design starts continue to rise as the semiconductor industry scales to a trillion dollars in revenue or more by the end of the decade. As the leading silicon-to-systems design solutions company with best-in-class EDA tools and the broadest portfolio of semiconductor IP, Synopsys' growth opportunity is truly incredible and already underway. Across industries, a paradigm shift is underway as companies race to deliver on this era of pervasive intelligence, where AI and smart technologies are omnipresent and interconnected. To capitalize on this shift, the technology industry is converging on a silicon-to-systems approach to innovation. As the company at the heart of silicon and systems, Synopsys was made for this moment – there is no one more capable of helping companies innovate for this new era of pervasive intelligence. Semiconductor companies are now designing with a system approach in mind, while systems companies are unlocking additional value through purpose-built chips and software-defined systems. At the same time, customers see the fusion of electronics design and physics simulation as critical to delivering high-performing and high-yielding solutions for their business.

Building on our seven-year partnership with Ansys, the industry leader in simulation, and a deliberate, multi-year strategy to reshape our business to support system-level design, last month we announced our intent to acquire Ansys. This transaction will grow our TAM by 1.5X to $28 billion and further enhance our silicon to systems strategy, both across our core EDA segment and in highly attractive adjacent growth areas where Ansys has an established presence and successful go-to-market expertise. Customer feedback on the proposed transaction has been incredibly supportive and we look forward to closing this transaction in the first half of 2025.

Now, I'll share some segment highlights starting with Design Automation, where we saw strong design win activity across the business. We continue to enhance our leadership in digital EDA as our capabilities become increasingly critical for the leading chips at advanced nodes. We are proud to have partnered with our customers to achieve a number of industry firsts in Q1: the world's first GAA-based next generation ARM Cortex-X mobile core tapeout at a leading Asian mobile SoC provider, the first completed tapeout for a server SoC on 18A, and Asia's first N5A ARM flagship automotive core tapeout for a leading EV OEM. In addition, we had multiple competitive wins, anchored by 2nm and 3nm projects at a leading Asian mobile semiconductor company. We are also gaining momentum with analog/mixed signal customers. We won several competitive full-flow displacements at analog/mixed signal companies, including networking OEMs in Europe and Japan.

A key differentiator in these competitive wins was the breadth and leadership of our EDA platform, from digital to analog and from architecture to signoff, all turbo-charged with the industry's leading full-flow AI platform, Synopsys.ai. Synopsys.ai focuses on three distinct pillars of value for our customers: optimization – XSO.ai, data analytics – X.da, and generative AI, including our Copilot. Starting with our XSO.ai family which includes design, verification, test and analog space optimization. We continue to expand our footprint and drive sell-up in our core EDA tools. DSO.ai was key in several major wins and continues to drive a 20% plus uplift to Fusion Compiler revenue at multiple accounts. Increasing share of usage of DSO.ai versus the competition was driven by superior PPA results on our platform versus alternatives. We saw very strong pull for VSO.ai with multiple production deployments that are seeing excellent improvements in test coverage and turn-around-time. A large North American HPC semiconductor company made a significant investment in VSO.ai technology with plans to immediately deploy on 4 projects and eventually deploy corporate-wide. Another large North American GPU company saw 2X faster turn-around-time and a 20% improvement in coverage and is planning a large-scale deployment of the technology. Our analog AI tool, ASO.ai, now has multiple deployments moving to production with reference flows at TSMC, Samsung and Intel for analog migration. We also broadened the capability of TSO.ai, adding a design-for-test feature to the proven ability for advanced pattern generation. At the International Test Conference this quarter, we demonstrated a 20% reduction in total pattern count using TSO.ai. Our data analytics AI products also saw significant logo engagement growth. A great example is Silicon.da production analytics, which is part of the Silicon Lifecycle Management family, and spans design through product manufacturing phases. Silicon.da automatically highlights silicon data outliers, enabling engineering teams to quickly identify and correct underlying issues in design and manufacturing and boost productivity. Last quarter, we had a groundbreaking generative AI announcement with Microsoft for accelerating chip design, Synopsys.ai Copilot. The integration of

GenAI across Synopsys.ai provides chip designers with collaborative capabilities that offer expert tool guidance, generative capabilities to enable RTL and collateral creation from natural language. Following positive feedback from initial pilot participants: AMD, Intel and Microsoft, we'll be adding a number of other companies with our beta roll-out.

In Q1, we also won significant multi-die package designs. Our 3DIC Compiler platform gained substantial momentum in multi-die packaging. Multi-die implementations continue to increase in the HPC market with an expectation that by 2028, 40% of HPC designs will be multi-die architectures. Like the transition to AI, this new design paradigm will create significant opportunity for both our EDA and IP businesses.

Moving to our systems business. Hardware-assisted verification had a strong quarter with excellent bookings on Zebu and HAPS across multiple geos with 8 new hardware logos. We saw share expansion at a large Asian OEM on Zebu 5 and grew our HAPS footprint at 2 top North American customers. In Systems Software, bookings momentum continued with key automotive OEMs and Tier 1s. One example was the collaboration we announced with Continental. Integrating our industry-leading virtual prototyping solutions within Continental's Automotive Edge development framework, we're building the digital twin capabilities that allow automakers to accelerate their software development and improve their time to market.

Now moving to Design IP, which continues to deliver industry-leading growth as the IP supplier of choice for leading HPC, AI, automotive and mobile chips at advanced nodes. This quarter, we closed a multi-year, multi-node and multi-foundry agreement to enable next generation Automotive and IoT platforms in a landmark design win at a major North American semiconductor company. A keystone IP in HPC and AI is PCIe 6.0 where we lead the industry with more than 50 lifetime wins. We demonstrated our next wave of innovation, by showcasing our PCIe 7.0 technology at DesignCon 2024. Multi-die packaging is a significant tailwind to IP as well as EDA. We won 4 die-to-die IP engagements in the quarter, surpassing 45 lifetime, enhancing our leadership in this emerging space. We proudly demonstrated the industry's first silicon success for UCIe S PHY IP in TSMC N3E and N5.
The tight integration with our flagship EDA tool, 3DIC Compiler, is generating significant productivity gains with improved design margins. Finally, at the beginning of the quarter we launched our new ARC-V RISC-V based portfolio with strong customer interest. The ARC-V processors are highly configurable and extensible to deliver optimal power-performance efficiency for a broad range of applications such as automotive, storage and IoT.

Now, to the Software Integrity segment, which delivered record revenue despite a challenging macroeconomic backdrop for enterprise software. We continue to evaluate strategic alternatives for this business, and we will provide an update when we complete this process. While the company engages in this process, the Software Integrity Group will continue to focus on investing and innovating in our market-leading products and serving customers with our leading application security testing portfolio and a global go-to-market execution.

In summary, we had an excellent start to the year, building on momentum underpinned by multiple secular growth drivers. We have a resilient business model, and our customers continue to prioritize investments in the silicon and systems that position them for future growth. We are aligning our portfolio investment with the greatest return potential to accelerate our growth. Thank you to our employees, partners and customers for their passion and commitment. Finally, we look forward to providing you more insight into our business, strategy and growth opportunities at our upcoming Investor Day, which will be held in conjunction with our Synopsys User's Group Event in Santa Clara on March 20th. I hope to see many of you there. With that, I'll turn it over to Shelagh.

Thank you, Sassine. We delivered a solid start to the year, with revenue in the upper end of our guided range, non-GAAP operating margin of 38.7%, and non-GAAP earnings above the high end of our guidance range. Our Q1 results are driven by our execution and leadership position across our segments, robust design activity across semiconductor and systems customers, and the stability and resilience of our time-based business model. We remain confident in our business, and as a result, we are reaffirming our full-year 2024 targets for revenue and non-GAAP operating margin and raising our non-GAAP EPS guidance.

I'll now review our first quarter results. All comparisons are year-over-year, unless otherwise stated. We generated total revenue of $1.65 billion. Total GAAP costs and expenses were $1.29 billion. Total non-GAAP costs and expenses were $1.01 billion, resulting in a non-GAAP operating margin of 38.7%. GAAP earnings per share were $2.89, and non-GAAP earnings per share were $3.56. Q1 included an extra fiscal week, which contributed $70.5 million in revenue and $0.11 in non-GAAP EPS. Now, onto our segments. Design Automation segment revenue was $985.3 million, up 11%. Design Automation adjusted operating margin was 37.0%. Design IP segment revenue was $525.7 million, up 53%, driven by broad-based strength. Design IP adjusted operating margin was 47.5%. Software Integrity revenue was $138.2 million, up 8%, and adjusted operating margin was 17.3%. Operating cash outflow was $88 million for the quarter, and we ended the quarter with cash and short-term investments of $1.27 billion.

Now to guidance. For fiscal year 2024, the full year targets are revenue of $6.57 to $6.63 billion; total GAAP costs and expenses between $5.02 and $5.08 billion; total non-GAAP costs and expenses between $4.14 and $4.18 billion; resulting in non-GAAP operating margin improvement of roughly 2 percentage points; non-GAAP tax rate of 15%; GAAP earnings of $9.56 to $9.74 per share; non-GAAP earnings of $13.47 to $13.55 per share; cash flow from operations of approximately $1.4 billion. Now to the targets for the second quarter: revenue between $1.56 and $1.59 billion; total GAAP costs and expenses between $1.21 and $1.23 billion; total non-GAAP costs and expenses between $1.01 and $1.02 billion; GAAP earnings of $2.05 to $2.16 per share; and non-GAAP earnings of $3.09 to $3.14 per share. Our press release and financial supplement include additional targets and GAAP to non-GAAP reconciliations.

In conclusion, we delivered a solid start to the year. We continue to execute, and for the year, expect 12.4-13.5% revenue growth, non-GAAP operating margin improvement of roughly 2 percentage points, and 20-21% non-GAAP EPS growth. Our confidence reflects our leadership position across our segments, robust design activity by our customers, and the stability and resiliency of our time-based business model. With that, I'll turn it over to the operator for questions.